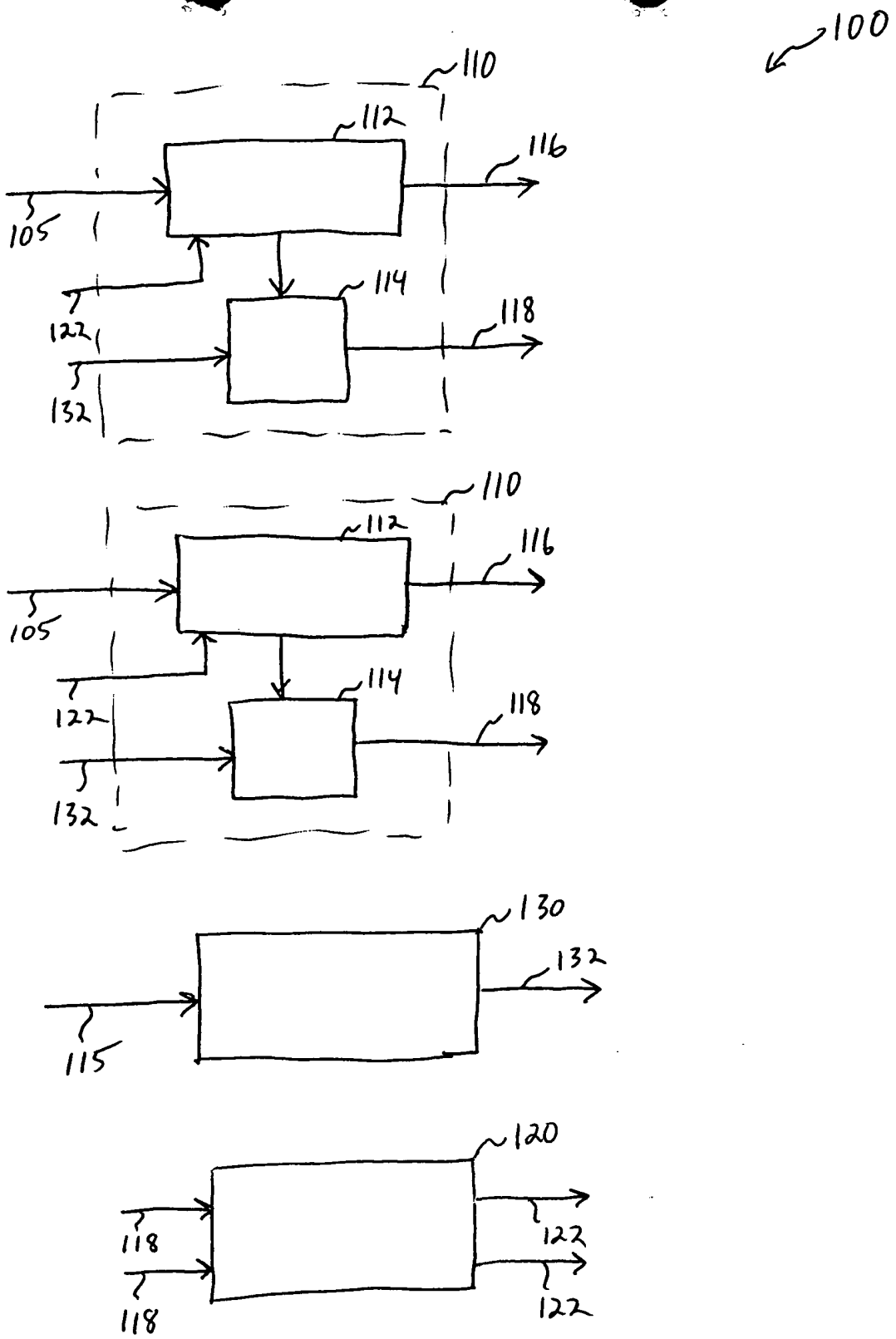
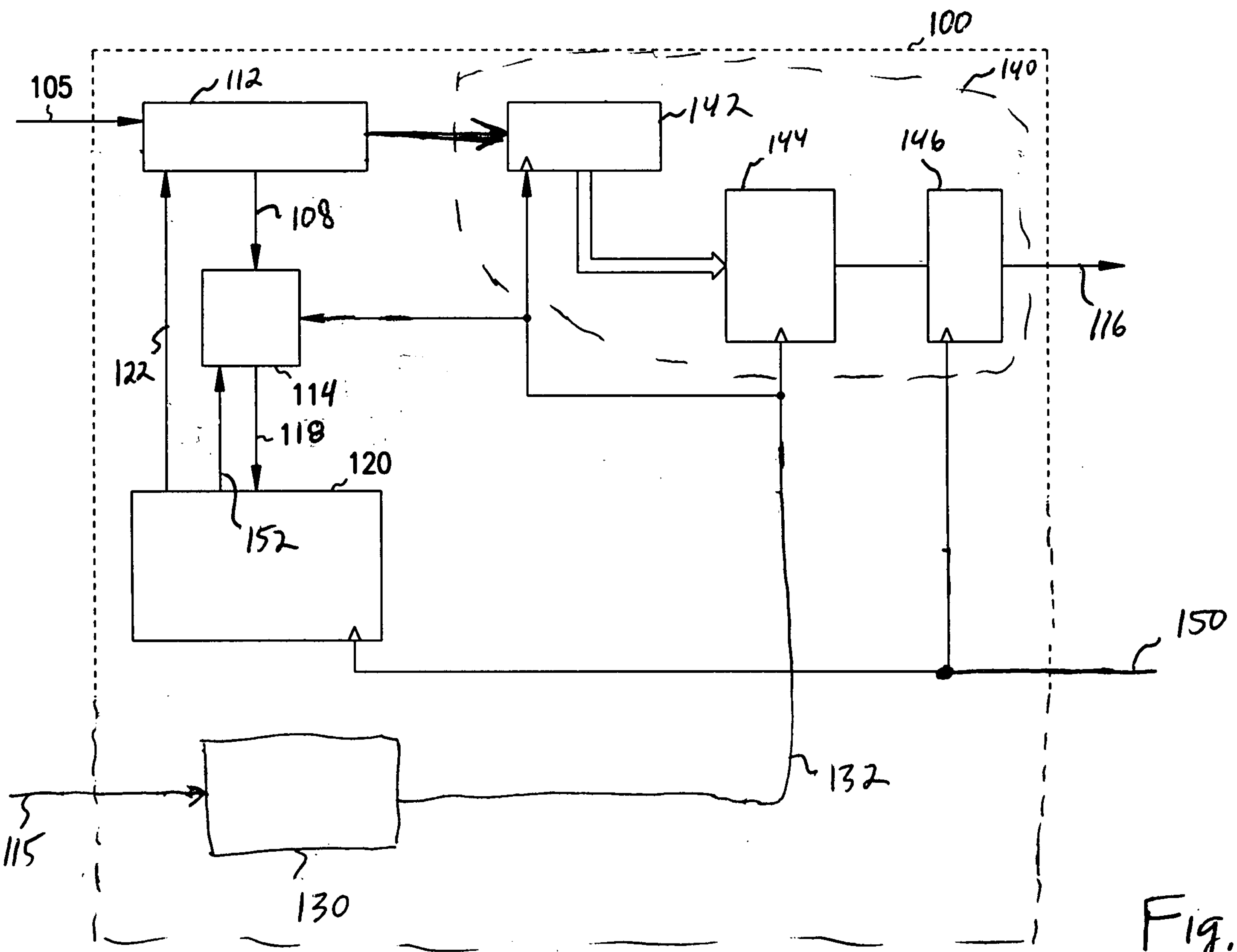

100
110
112
116
105
114
118
122
132
110
112
116
105
114
118
122
132
130
132
115
120
118
118
122
122

Fig. 1



100
105
112
142
140
144
146
108
116
122
114
118
120
152
150
132
115
130

Fig. 2

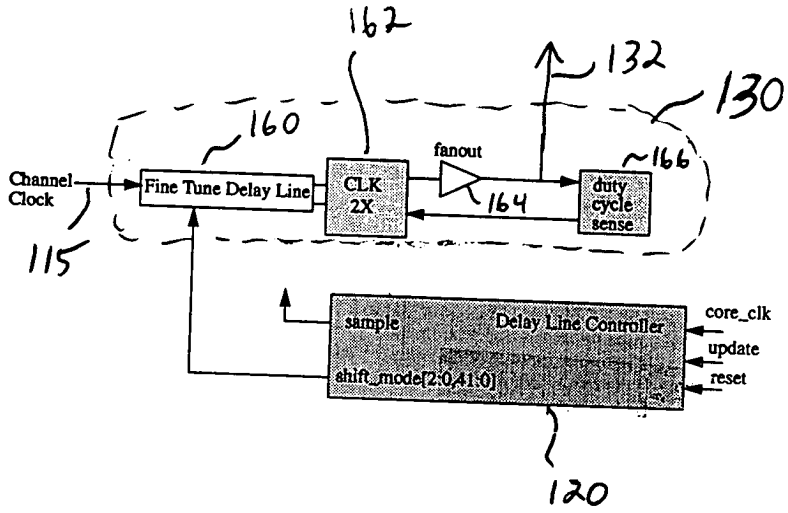

162
132
130
160
fanout
166
Channel Clock
Fine Tune Delay Line
CLK 2X
164
duty cycle sense
115
sample
Delay Line Controller
core_clk
update
reset
shift_mode[2:0,41:0]
120

Fig. 3

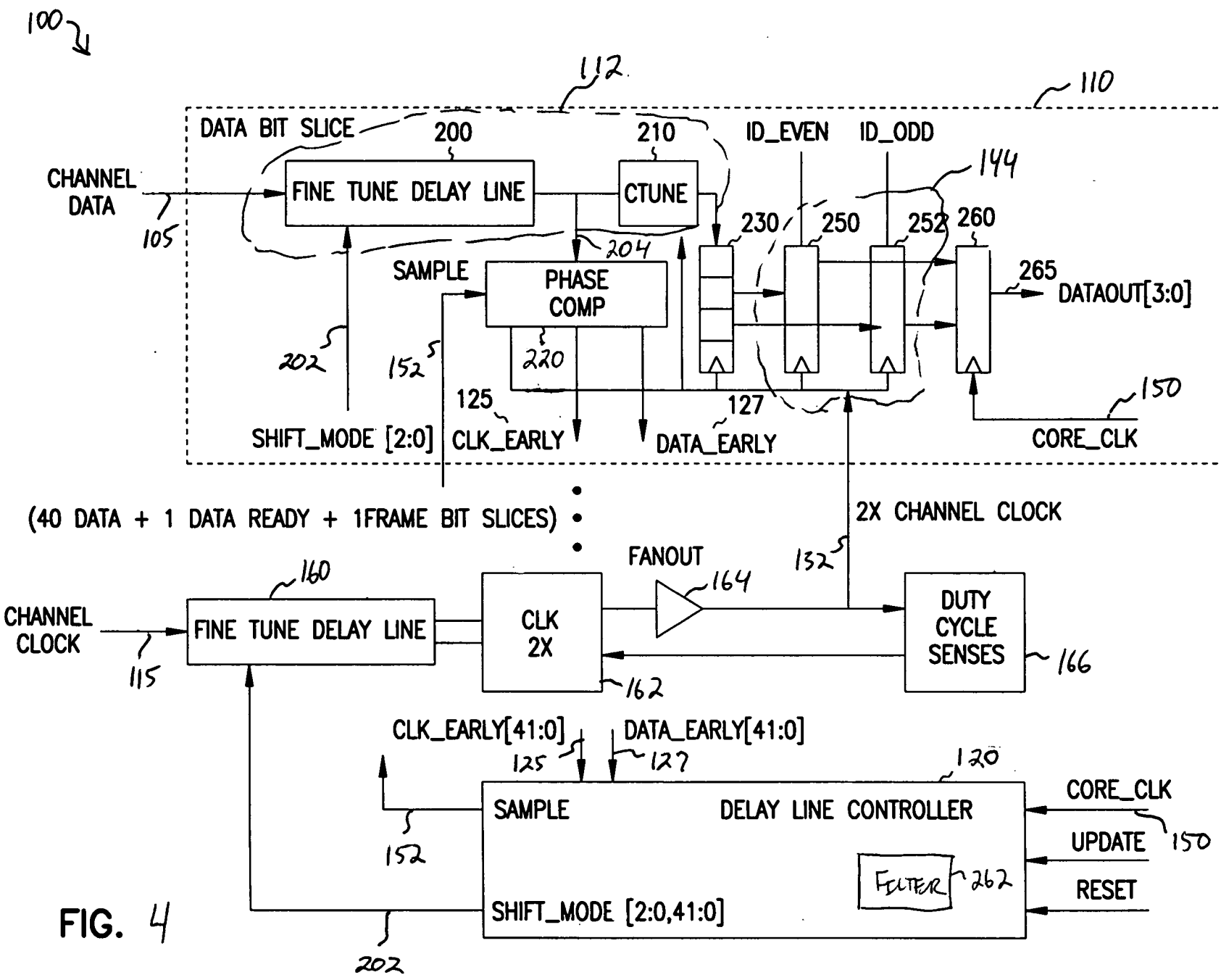


FIG. 4

FIGURE 14. PFSSR Timing Diagram

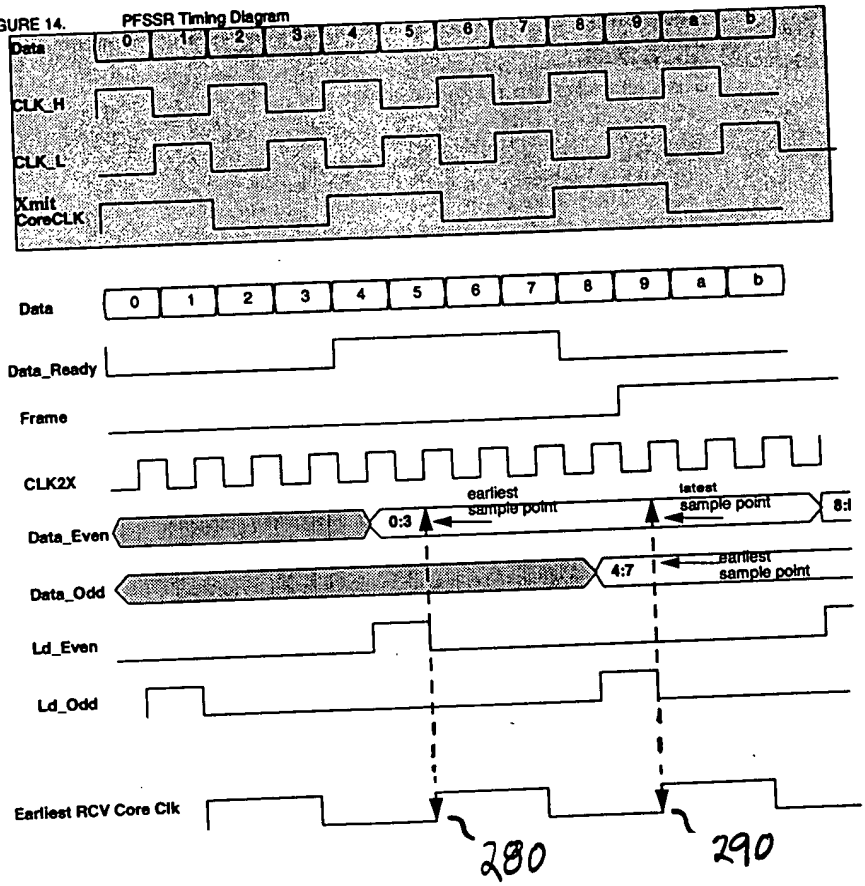


Fig. 5

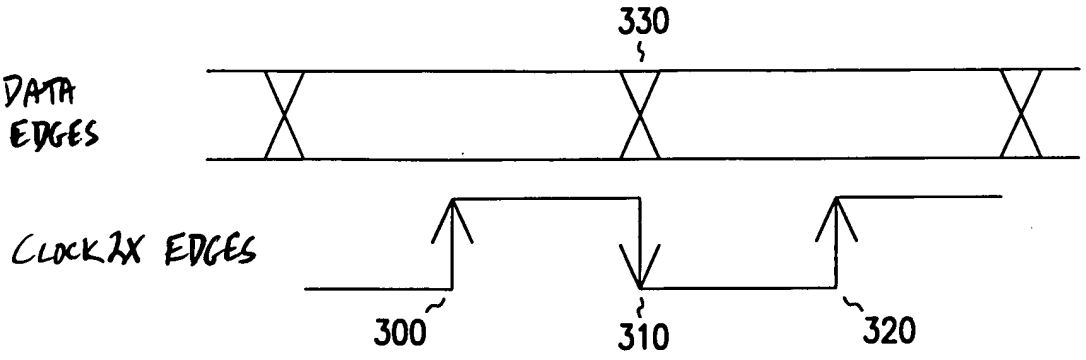

330
DATA EDGES
CLOCK2X EDGES
300
310
320

FIG. 6

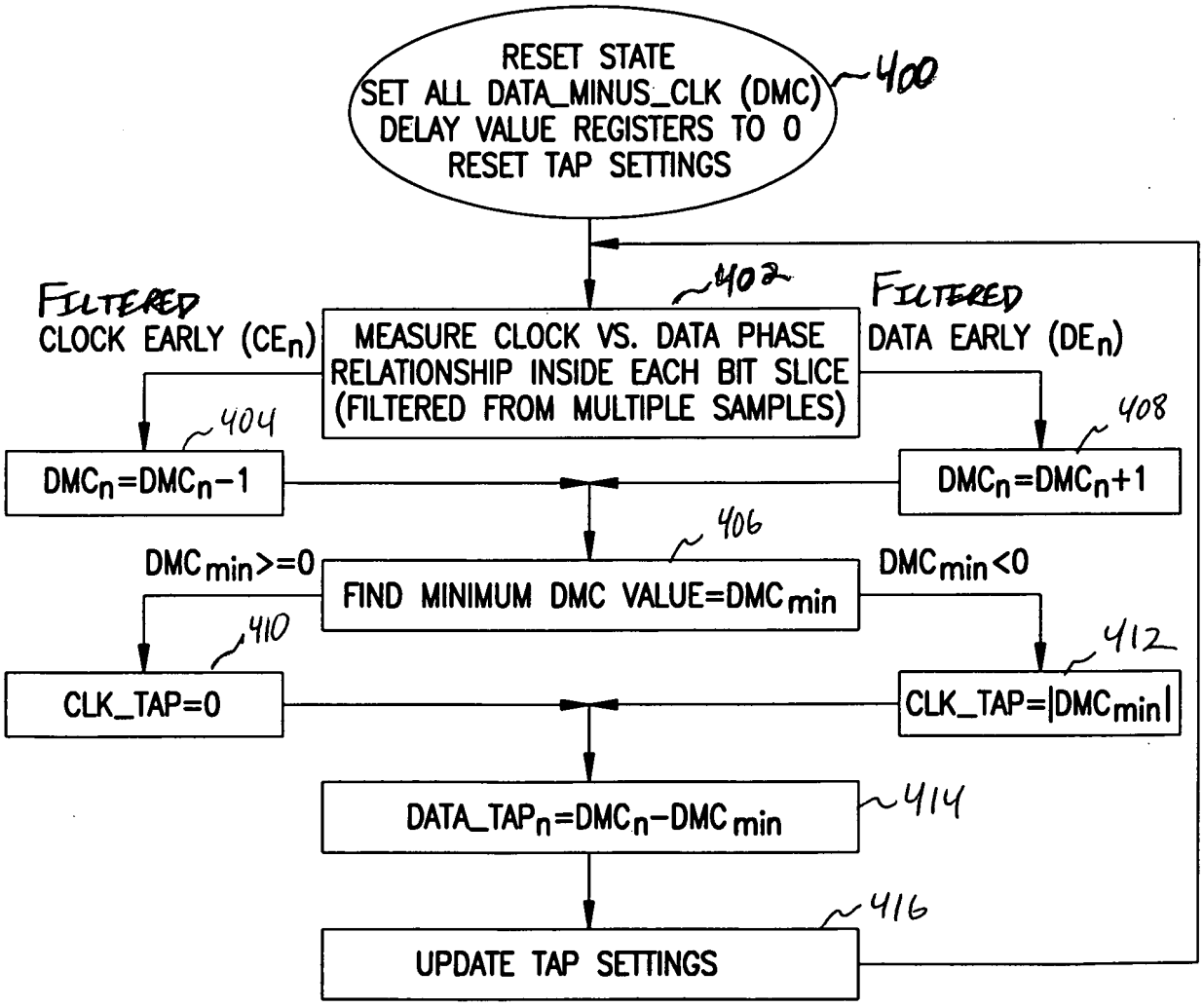

RESET STATE
SET ALL DATA_MINUS_CLK (DMC) DELAY VALUE REGISTERS TO 0
RESET TAP SETTINGS
400
402
MEASURE CLOCK VS. DATA PHASE RELATIONSHIP INSIDE EACH BIT SLICE (FILTERED FROM MULTIPLE SAMPLES)
FILTERED CLOCK EARLY (CEn)
FILTERED DATA EARLY (DEn)
404
DMCn=DMCn-1
408
DMCn=DMCn+1
406
DMCmin>=0
FIND MINIMUM DMC VALUE=DMCmin
DMCmin<0
410
CLK_TAP=0
412
CLK_TAP=|DMCmin|
DATA_TAPn=DMCn-DMCmin
414
416
UPDATE TAP SETTINGS

FIG. 9

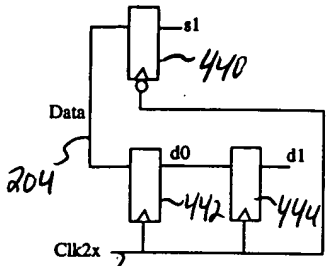


Fig. 8a

Possible Samples - condition

d1	s1	d0	condition
0	0	0	steady 0 (no timing info.)
0	0	1	rising data (clk early)
0	1	0	(uncertain sample)
0	1	1	rising data (data early)
1	0	0	falling data (data early)
1	0	1	(uncertainsample)
1	1	0	falling data (clk early)
1	1	1	steady 1 (no timing info.)

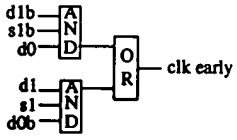


Fig. 8b

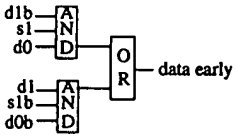


Fig. 8c

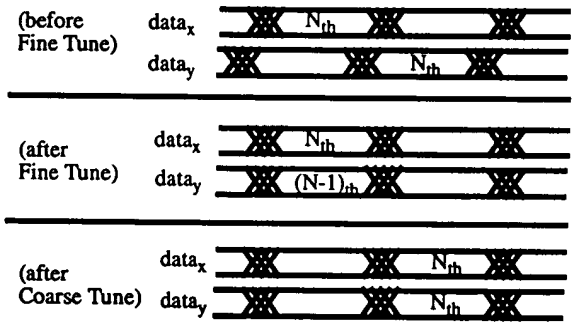


Fig. 7

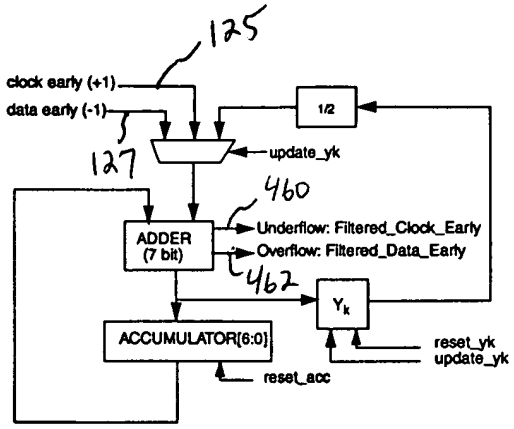

125
clock early (+1)
data early (-1)
127
1/2
update_yk
460
ADDER
(7 bit)
Underflow: Filtered_Clock_Early
Overflow: Filtered_Data_Early
462
Y_k
ACCUMULATOR[6:0]
reset_yk
update_yk
reset_acc

Fig. 10

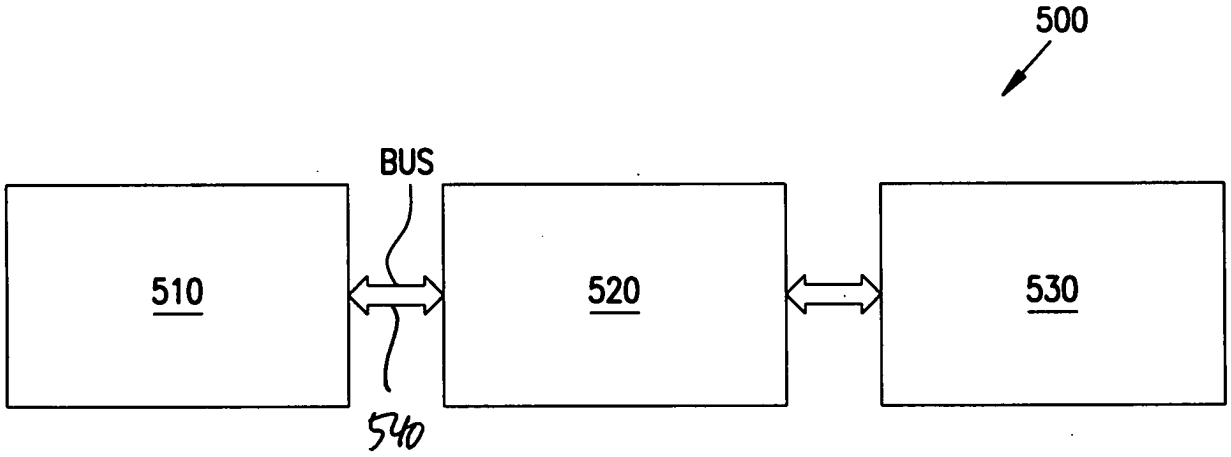


FIG. 11